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N-bit control number, with N being an integer greater than 1,
said oscillator comprising

a first group of cells, each cell comprising at
least one inverter,

a first selection circuit connected to said
first group of cells for selecting a number of cells
as a function of predetermined most significant bits
of (the control number),

a second group of cells, each cell comprising
at least one inverter, and

a second selection circuit connected to said
second group of cells for selecting one of the cells
within said second group of cells as a function of
predetermined least significant bits of (the control
number)

selected cells of said first and second groups
being connected in series to form a chain of
inverters.

19. A signal generator according to Claim 18,
wherein each cell within said second group of cells is
assigned a place value j ranging from 1 to NL.

20. A signal generator according to Claim 19,
wherein said second selection circuit comprises NL switches
controlled by signals representing the least significant bits
of (the control number) each switch being series connected with
a cell having a same place value j between an input and an
output of the second group of cells.

21. A signal generator according to Claim 18,

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wherein two different cells within said second group of cells have different propagation times for a first logic value and a second logic value.

22. A signal generator according to Claim 19, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within said second group of cells having a place value j and that of a cell within said second group of cells having a place value $j-1$ is less than a desired uncertainty for a period of the output signal.

23. A signal generator according to Claim 19, wherein when (the control number) increases by 1, a cell within said second group of cells with a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within said second group of cells, and a cell with a lower place value, with an additional cell within said first group of cells also being selected.

24. A signal generator according to Claim 18, further comprising a comparator for comparing a period of the output signal with a desired period for providing the N-bit control number in the form of N logic signals, with (the control number) increasing if the period of the output signal is less than the desired period, decreasing if the period of the output signal is larger than the desired period, and remaining constant otherwise.

25. A signal generator according to Claim 19,

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further comprising a first decoder for decoding the least significant bits NL0 of (the control number) and for providing a first set $NL = 2^{NL0}$ of control signals (SDL(1) to SDL(NL)) to said second selection circuit, this first set of control signals having the following properties: $SDL(j) = 1$ if $j = NRL+1$ for any value of j ranging from 1 to NL, with NRL corresponding to a decimal value of the NL0 least significant bits of (the control number). 9

26. A signal generator according to Claim 25, further comprising a second decoder for decoding the most significant bits NH0 of (the control number) and for providing said first selection circuit a second set $NH = 2^{NH0}$ of control signals (SDH(1) to SDH(NH)), this second set of control signals having the following properties: $SDH(i) = 1$ if $i = NRH+1$ for any value of i ranging from 1 to NH, with NRH corresponding to a decimal value of the NH0 most significant bits of (the control number). A

27. A signal generator according to Claim 18, further comprising a control circuit for verifying the following inequality and producing a first control signal if the inequality is not verified:

$$0 \leq (TC0+TC1) + (TD0(1)+TD1(1)) - (TD0(NL)+TD1(NL))$$

wherein:

TC0+TC1 is a propagation time of a first logic value and a second logic value in a cell within said first group of cells,

TD0(1)+TD1(1) is a propagation time of a first

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logic value and a second logic value in a least significant cell within said second group of cells, and

$TD0(NL)+TD1(NL)$ is a propagation time of a first logic value and a second logic value in a most significant cell within said second group of cells.

28. A signal generator according to Claim 27, wherein said control circuit comprises:

a reference oscillator for providing a signal with a reference period proportional to $(TC0+TC1) + (TD0(1)+TD1(1))$;

a first measurement oscillator for providing a signal having a measured period proportional to $(TD0(NL)+TD1(NL))$; and

a first comparison circuit for comparing the measured period with a reference period and for providing (the first control signal) if the measured period is smaller than the reference period. 10

29. A signal generator according to Claim 27, further comprising a comparator for comparing a period of the output signal with a desired period for providing the N-bit control number in the form of N logic signals, and said comparator increases the N-bit control number by one unit when the control signal is received.

30. A signal generator according to Claim 28, wherein said control circuit further comprises:

a second measurement oscillator for providing a signal having a second measured period proportional to $(TD0(NL-1)+TD1(NL-1))$; and

a second comparison circuit for comparing (the second

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period) with the reference period, and for providing a second control signal if the measured period is less than the reference period.

31. A signal generator according to Claim 30, wherein said control circuit is activated when said oscillator starts to operate, and at least one of the first and second control signals is memorized.

32. A signal generator according to Claim 31, wherein the first control signal is taken into account when the cell with the place value NL-1 within said second group of cells is selected.

33. A signal generator according to Claim 31, wherein the second control signal is taken into account when the cell with the place value NL-2 within said second group of cells is selected.

34. A signal generator according to Claim 31, wherein said control circuit is activated when the cell with the place value NL-1 within the second group of cells is selected.

35. A signal generator according to Claim 31, wherein said control circuit is activated when the cell with the place value NL-2 within said second group of cells is selected.

36. A signal generator comprising:
a comparator for comparing a period of an output

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signal with a desired period for providing an N-bit control number;

a first decoder for decoding predetermined least significant bits of the N-bit control number and for providing a first set of control signals;

a second decoder for decoding predetermined most significant bits of the N-bit control number and for providing a second set of control signals; and

an oscillator for providing the output signal from the N-bit control number, with N being an integer greater than 1, said oscillator comprising

a first group of cells, each cell comprising at least one inverter,

a first selection circuit connected to said first group of cells for selecting a number of cells based upon the second set of control signals,

a second group of cells, each cell comprising at least one inverter, and

a second selection circuit connected to said second group of cells for selecting one of the cells based upon the first set of control signals, each cell within said second group of cells being assigned a place value j ranging from 1 to NL,

selected cells of (said first and second groups) ^{no} ₂₆ being connected in series to form a chain of inverters.

37. A signal generator according to Claim 36, wherein said second selection circuit comprises NL switches controlled by the first set of control signals.

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38. A signal generator according to Claim 36, wherein two different cells within said second group of cells have different propagation times for a first logic value and a second logic value.

39. A signal generator according to Claim 36, wherein the control number increases if the period of the output signal is less than the desired period, decreases if the period of the output signal is larger than the desired period, and remains constant otherwise.

40. A signal generator according to Claim 36, further comprising a control circuit for verifying the following inequality and producing a first control signal if the inequality is not verified:

$$0 \leq (TC0+TC1) + (TD0(1)+TD1(1)) - (TD0(NL)+TD1(NL))$$

wherein:

TC0+TC1 is a propagation time of a first logic value and a second logic value in a cell within said first group of cells,

TD0(1)+TD1(1) is a propagation time of a first logic value and a second logic value in a least significant cell within said second group of cells, and

TD0(NL)+TD1(NL) is a propagation time of a first logic value and a second logic value in a most significant cell within said second group of cells.

41. A signal generator according to Claim 40, wherein said control circuit comprises:

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a reference oscillator for providing a signal with a reference period proportional to $(TC0+TC1) + (TD0(1)+TD1(1))$;

a first measurement oscillator for providing a signal having a measured period proportional to $(TD0(NL)+TD1(NL))$; and

a first comparison circuit for comparing the measured period with a reference period and for providing the first control signal if the measured period is smaller than the reference period.

42. A signal generator according to Claim 41, wherein said control circuit further comprises:

a second measurement oscillator for providing a signal having a second measured period proportional to $(TD0(NL-1)+TD1(NL-1))$; and

a second comparison circuit for comparing the second period with the reference period, and for providing a second control signal if the measured period is less than the reference period.

43. An oscillator for providing an output signal from an N-bit control number, with N being an integer greater than 1, the oscillator comprising:

a first group of cells, each cell comprising at least one inverter;

a first selection circuit connected to said first group of cells for selecting a number of cells as a function of predetermined most significant bits of the control number;

a second group of cells, each cell comprising at least one inverter; and

a second selection circuit connected to said second

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group of cells for selecting one of the cells as a function of predetermined least significant bits of (the control number) 13
the selected cells of said first and second groups being connected in series to form a chain of inverters.

44. An oscillator according to Claim 43, wherein each cell within said second group of cells is assigned a place value j ranging from 1 to NL , and wherein said second selection circuit comprises NL switches controlled by signals representing (the least significant bits) of (the control number) 5 each switch for being connected in series between an input and an output of a cell having a same place value j .

45. An oscillator according to Claim 43, wherein two different cells of said second group of cells have different propagation times for a first logic value and a second logic value.

46. An oscillator according to Claim 43, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within said second group of cells with a place value j and that of a cell within said second group of cells with a place value $j-1$ is less than a desired uncertainty for a period of the output signal.

47. An oscillator according to Claim 43, wherein when the control number increases by 1, a cell within said second group of cells with a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within said second group of cells, and a cell with a

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lower place value, with an additional cell within said first group of cells also being selected.

48. A method for generating an output signal comprising:

comparing a period of the output signal with a desired period for providing an N-bit control number;

decoding least significant bits of the N-bit control number for providing a first set of control signals; ✓

decoding most significant bits of the N-bit control number for providing a second set of control signals; and

providing the output signal based upon the N-bit control number, with N being an integer greater than 1, using an oscillator comprising a first group of cells, each cell comprising at least one inverter and a first selection circuit ✓ connected to the first group of cells, and a second group of ✓ cells, each cell comprising at least one inverter and a second selection circuit connected to the second group of cells, (the providing) comprising

selecting a number of cells within the first group of cells based upon the second set of control ✓ signals, and

selecting one of the cells within the second group of cells based upon the first set of control ✓ signals,

the selected cells of (the first and second groups) being connected in series to form a chain of inverters. —

49. A method according to Claim 48, wherein each cell within the second group of cells is assigned a place

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value j ranging from 1 to NL, and wherein the second selection circuit comprises NL switches controlled by the first set of control signals. ✓

50. A method according to Claim 48, wherein two different cells within the second group of cells have different propagation times for a first logic value and a second logic value.

51. A method according to Claim 48, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within the second group of cells having a place value j and that of a cell within the second group of cells having a place value j-1 is less than a desired uncertainty for a period of the output signal.

52. A method according to Claim 48, wherein when (the control number increases by 1, a cell within the second group of cells having a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within the second group of cells, and a cell with a lower place value, with an additional cell within the first group of cells also being selected.

53. A method according to Claim 48, wherein the control number increases if the period of the output signal is less than (the desired period), decreases if the period of the output signal is larger than (the desired period), and remains constant otherwise.